AP
IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

FENG CHEN

Serial No. 10/661,287 (TI-35766)

Filed September 12, 2003

CERTIFICATE OF MAILING OR TRANSMISSION UNDER 37 CFR 1.8

I hereby certify that the attached document is being deposited with the United States Postal Service with sufficient postage for First Class Mail in an envelope addressed to Director of the United States Patent and Trademark Office, P.O. Box 1450,, Alexandria, VA 22313-1450 or is being facsimile transmitted on the date indicated below:

9-5-06

Jay M. Cantor, Reg. No. 19,906

For: SIGMA-DELTA MODULATOR USING A PASSIVE FILTER

Art Unit 2819

Examiner Howard L. Williams

Customer No. 23494

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

REVISED BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 1 to 4, 6 to 12 and 14 to 17, all of the rejected claims. Claims 5, 13 and 18 to 20 have been allowed. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was not filed after a second or subsequent rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to a structure and method of operating a sigma-delta modulator. The structure as set forth in claim 1 has, in combination, as shown in Fig. 2, a digital feedback signal source (C_{R1})(page 10, line 17ff) for providing a digital feedback signal; a passive discrete time circuit (14)(page 7, line 1ff, page 10, line 17ff) for receiving the digital feedback signal and an input signal (V_{INP}, V_{INM} and 12), the input signal comprising information and a pair of analog input currents; converting the digital feedback signal into an analog feedback signal during a first discrete time (ϕ_1 and page 7, lines to 11) and summing the analog feedback signal and a selected one of the pair of analog input currents during a second discrete time (ϕ_2)(page 10, line 25ff) to yield a summed signal (page 7, lines 14 to 21). A passive continuous time circuit (16)(page 7, line 29ff and page 11, line 17ff) comprising a plurality of passive resistive and capacitive elements is coupled to the discrete time circuit to filter the summed signal using a first first-order filter containing resistive and capacitive elements (14 + 24)(page 11, line 16ff) serially connected to a second first order filter (26) containing resistive and capacitive elements to form a second first order filter to generate a filtered signal, the first-order filters comprising one or more first passive elements of the plurality of passive elements. A quantizer (18)(page 8, line 25ff) is coupled to the continuous time circuit to generate the digital signal using the filtered signal, the digital signal comprising the information. The digital signal determines the selected one of the pair of input signals (page 10, lines 25ff).

The method, as set forth in claim 9 requires the steps of providing a passive discrete time circuit (14)(page 7; line 1ff, page 10, line 17ff), at the passive discrete time circuit (a) receiving a

digital feedback signal and a pair of input signals (C_{R1}, V_{INP}, V_{INM})(page 10, line 1ff), the input signals comprising information and analog input currents (b) converting the digital feedback signal into an analog feedback signal during a first discrete time (ϕ_1 and page 7, lines to 11) and (c) summing the analog feedback signal and a selected one of the analog input currents during a second discrete time to yield a summed signal (ϕ_2)(page 10, line 17ff), providing a passive continuous time circuit (16)(page 7, line 29ff, page 11, line 17ff), at the passive continuous time circuit (a) filtering the summed signals at a continuous time circuit in order to generate a filtered signal (page 11, lines 16ff), the continuous time circuit comprising a first passive first-order filter (14 + 24) and a second passive first order filter (26)(page 11, line 16ff), the first first-order filter comprising one or more first passive resistive and capacitive elements of the plurality of passive elements, the second first order filter comprising one or more second passive resistive and capacitive elements of the plurality of passive elements and (b) generating the digital signal using the filtered signals, the digital signal comprising the information, said digital signal determining the selected one of said pair of input signal (18)(page 8, line 25ff and page 13, line 3ff).

The structure, as set forth in means plus function recitation in claim 17, requires means for receiving a digital feedback signal and a pair of analog input signals at a discrete time circuit (C_{R1}, V_{INP}, V_{INM})(page 10, line 1ff), the input signal comprising information and analog input currents, means for converting the digital feedback signal into an analog feedback signal during a first discrete time (ϕ_1 and page 7, lines to 11), means for summing the analog feedback signal and a selected one of said pair of analog input currents during a second discrete time to yield a summed signal (ϕ_2)(page 10, line 17ff), means for filtering the summed signals at a continuous time circuit in order to generate a filtered signals, the continuous time circuit comprising a first

passive first-order filter and a passive second passive first order filter, each filter containing both resistive and capacitive elements (16 and elements 14 + 24 and 26)(page 7, line 29ff and page 11, line 17ff and means for generating the digital signal using the filtered signal, the digital signal comprising the information, said digital signal determining the selected one of said pair of input signals (18)(page 8, line 25ff).

The sigma delta modulator can further comprise a transconductance circuit (12) to: receive the input signal comprising the information, the input signal having one or more analog input voltages; and convert the one or more analog input voltages into one or more analog input currents.

The discrete time circuit can convert the digital feedback signal into an analog feedback signal using a reference voltage (V_{REFP}, V_{REFM}), the reference voltage supplied by a reference capacitor (C_{R1}), the reference capacitor charged to the reference voltage during the first discrete time (Φ_1).

The one or more passive elements associated with the first first order filter can comprise a first capacitor (C_1) and the one or more passive elements associated with the second first order filter comprises a second capacitor and a resistor (C_2, R_2). The second capacitance and the resistance can be selected according to a frequency response, the frequency response corresponding to a direct current frequency.

The quantizer can comprise a comparator to generate the digital signal using the one or more filtered signals by amplifying the one or more filtered signals and comparing the one or more filtered signals to each other to quantize an error associated with the input signal and the digital signal (page 10, lines25 to page 11, line 4)..The output of the quantizer can be coupled to

the discrete time circuit in order to form a passive feedback loop, the passive feedback loop operable to convert the digital signal into an analog feedback signal.

GROUNDS OF REJECTION

Claims 1 to 4, 6 to 12, and 14 to 17 were rejected under 35 U.S.C.103(a) as being unpatentable over the Benabes et al. article (Passive sigma-delta converter design) in view of the Chen et al. article (A 0.25 mW Low-Pass Passive Sigma-Delta Modulator with Built-In Mixer for a 10 MHz IF Input) and Yamakido et al. (U.S. 5,227,795) or Voorman et al. (U.S. 5,103,228).

ARGUMENT

Claims 1 to 4, 6 to 12, and 14 to 17 were rejected under 35 U.S.C.103(a) as being unpatentable over the Benabes et al. article in view of the Chen et al. article and Yamakido et al. or Voorman et al. The rejection is without merit.

It is initially noted that the Chen et al. article is a reference authored by the applicant herein and is an improvement thereof. It is further noted that the allegation that Benabes et al. discloses passive filters in the first column (see first two paragraphs after INTRODUCTION in Benabes et al.) is that of a reference to the Chen et al. article wherein Bosco Leung was the secondary contributor. It follows that Benabes et al. do not teach the use of a totally passive circuit in their own structure but merely refer to art prior to their article where such a circuit is discussed. Furthermore, this feature, though inventive in its own right, is only of secondary importance in the present invention as will be demonstrated.

All of the rejected independent claims (claims 1, 9 and 17) require a pair of analog input currents with the selection of the one of the pair of input currents being responsive to the digital output of the quantizer. No such feature is taught or suggested by any of the cited references.

All of the claims require that both the discrete time circuit and the continuous time circuit be passive. Clearly, Benabes et al. nowhere teach or suggests the circuit as claimed either in structure format or in method format other than stating that a design for a passive sigma-delta converter is provided. The claims herein require much more. Claim 1, in addition to the feature discussed above, requires the combination of "a passive discrete time circuit for receiving the digital feedback signal and an input signal, the input signal comprising information and a pair of analog input currents; converting the digital feedback signal into an analog feedback signal during a first discrete time; and summing the analog feedback signal and a selected one of the pair of analog input currents during a second discrete time to yield a summed signal" and "a passive continuous time circuit comprising a plurality of passive resistive and capacitive elements, the continuous time circuit coupled to the discrete time circuit to filter the summed signal using a first first-order filter containing resistive and capacitive elements serially connected to a second first order filter containing resistive and capacitive elements to form a second first order filter to generate one or more filtered signals, the first-order filters comprising one or more first passive elements of the plurality of passive elements". The examiner has directed attention to Fig. 3 of Benabes et al. However, this figure is merely a showing of a filter using all passive elements. Claim 1 calls for much more. Not only does claim 1 require the combination of filters as claimed, but, in addition, claim 1 requires "a passive discrete time circuit for: receiving the ~~a~~ digital feedback signal and an input signal, the input signal comprising information and a pair of analog input currents; converting the digital feedback signal into an

analog feedback signal during a first discrete time; and summing the analog feedback signal and a selected one of the pair of analog input currents during a second discrete time to yield a summed signals" coupled to the passive continuous time circuit. No such circuit is taught or suggested by Benabes et al. either alone or in the combination as claimed.

As to the Chen et al. reference, while, as noted in the Office action, Benabes et al. refers to this publication, it is noted that the reference to Chen et al is with reference to "first order modulators" and nothing else. Clearly, Benabes et al. nowhere considered combining the circuit of Chen et al with their device. Furthermore, the circuit of Chen et al. nowhere teaches or suggests the specific features of the discrete time circuit as claimed, even were it combinable with Benabes et al., which it clearly is not. It is clear that Chen et al. was not only available to Benabes et al., but also fully considered by Benabes et al. as evidenced by the fact that Chen et al. is cited by Benabes et al. Despite this fact, is was not obvious to Benabes et al. to provide the combination now improperly devised by the examiner in hindsight, even were the combination to teach or suggest the invention claimed herein, which it does not as demonstrated herein..

As to Voorman et al., there is clearly no teaching or suggestion to combine this reference with Benabes et al. and Chen et al. other that from a first study of the subject disclosure.

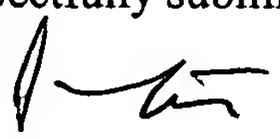
In summary, as to each of the rejected independent claims, these claims require a quantizer for generating a digital signal from the continuous time circuit, the digital signal determining the selection of one of the pair of input signals as well as the combination of the passive continuous time circuit in combination with a passive discrete time stage wherein the input signal and the feedback signal are combined. There is no teaching or suggestion in any of the references not only of such circuits, but also of such a combination. Even were the

individual circuits to be depicted in the prior art, some of which are not, the combination as claimed is nowhere taught or suggested by the applied prior art.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,



Jay M. Cantor
Reg. No. 19906
(301) 44-0355
(972) 917-5293

CLAIMS APPENDIX

The claims on appeal read as follows:

1. A sigma-delta modulator, comprising:

an digital feedback signal source for providing a digital feedback signal;

a passive discrete time circuit for receiving the digital feedback signal and an input signal, the input signal comprising information and a pair of analog input currents; converting the digital feedback signal into an analog feedback signal during a first discrete time; and summing the analog feedback signal and a selected one of said pair of analog input currents during a second discrete time to yield a summed signal;

a passive continuous time circuit comprising a plurality of passive resistive and capacitive elements, the continuous time circuit coupled to the discrete time circuit to filter the summed signal using a first first-order filter containing resistive and capacitive elements serially connected to a second first order filter containing resistive and capacitive elements to form a second first order filter to generate a filtered signals, the first-order filters comprising one or more first passive elements of the plurality of passive elements, and

a quantizer coupled to the continuous time circuit to generate the digital signal using the filtered signal, the digital signal comprising the information, said digital signal determining the selected one of said pair of input signals.

2. The sigma delta modulator of Claim 1, further comprising a transconductance circuit to: receive the input signals comprising the information and convert the analog input voltages into analog input currents.

3. The sigma-delta modulator of Claim 1, wherein the discrete time circuit converts the digital feedback signal into an analog feedback signal using a reference voltage, the reference voltage supplied by a reference capacitor, the reference capacitor charged to the reference voltage during the first discrete time.

4. The sigma-delta modulator of Claim 1, wherein:

the one or more passive elements associated with the first first order filter comprises a first capacitor; and

the one or more passive elements associated with the second first order filter comprises a second capacitor and a resistor.

6. The sigma-delta modulator of Claim 1, wherein:

the one or more passive elements associated with the second first order filter comprises a second capacitor and a resistor, the second capacitor associated with a second capacitance, the resistor associated with a resistance; and

the second capacitance and the resistance selected according to a frequency response, the frequency response corresponding to a direct current frequency.

7. The sigma-delta modulator of Claim 1, wherein the quantizer comprises a comparator to generate the digital signal using the filtered signals by:

amplifying the filtered signal; and

comparing the filtered signal to another filtered signal to quantize an error associated with the input signal and the digital signal.

8. The sigma-delta modulator of Claim 1, wherein the output of the quantizer is coupled to the discrete time circuit in order to form a passive feedback loop, the passive feedback loop operable to convert the digital signal into an analog feedback signal.

9. A method for converting an input signal into a digital signal, comprising the steps of:

providing a passive discrete time circuit;

at said passive discrete time circuit (a) receiving a digital feedback signal and a pair of input signals, the input signals comprising information and analog input currents; (b) converting the digital feedback signal into an analog feedback signal during a first discrete time; and (c) summing the analog feedback signal and a selected one of the analog input currents during a second discrete time to yield a summed signals;

providing a passive continuous time circuit;

at said passive continuous time circuit (a) filtering the summed signals at a continuous time circuit in order to generate a filtered signals, the continuous time circuit comprising a first passive first-order filter and a second passive first order filter, the first first-order filter comprising one or more first passive resistive and capacitive elements of the plurality of passive elements, the second first order filter comprising one or more second passive resistive and capacitive elements of the plurality of passive elements; and (b) generating the digital signal using the filtered signals, the digital signal comprising the information, said digital signal determining the selected one of said pair of input signals.

10. The method of Claim 9, further comprising:

receiving at a transconductance circuit the input signal comprising the information, the input signal having said pair of analog input voltages; and

converting the analog input voltages into the one or more analog input currents.

11. The method of Claim 9, wherein converting the digital feedback signal into an analog feedback signal during the first discrete time further comprises using a reference voltage, the reference voltage supplied by a reference capacitor, the reference capacitor charged to the reference voltage during the first discrete time.

12. The method of Claim 9, wherein:

the one or more first passive elements associated with the first first order filter comprises a first capacitor; and

the one or more second passive elements associated with the second first order filter comprises a second capacitor and a resistor.

14. The method of Claim 9, wherein:

the one or more second passive elements associated with the second first order filter comprises a second capacitor and a resistor, the second capacitor associated with a second capacitance, the resistor associated with a resistance; and

the second capacitance and the resistance selected according to a frequency response, the frequency response corresponding to a direct current frequency.

15. The method of Claim 9, wherein generating the digital signal using the one or more filtered signals further comprises:

amplifying the filtered signals; and

comparing at a comparator the filtered signals to another filtered signal to quantize an error associated with the input signal and the digital signal.

16. The method of Claim 9, wherein the output of the quantizer is coupled to the discrete time circuit to form a passive feedback loop, the passive feedback loop converting the digital signal into an analog feedback signal.

17. A sigma-delta modulator, comprising:

means for receiving a digital feedback signal and a pair of analog ~~an~~ input signals at a discrete time circuit, the input signal comprising information and analog input currents;

means for converting the digital feedback signal into an analog feedback signal during a first discrete time;

means for summing the analog feedback signal and a selected one of said pair of analog input currents during a second discrete time to yield a summed signal;

means for filtering the summed signals at a continuous time circuit in order to generate a filtered signals, the continuous time circuit comprising a first passive first-order filter and a passive second passive first order filter, each filter containing both resistive and capacitive elements; and

means for generating the digital signal using the filtered signal, the digital signal comprising the information, said digital signal determining the selected one of said pair of input signals.

EVIDENCE APPENDIX

Not applicable

RELATED PROCEEDINGS APPENDIX

Not applicable